# VLSI Test Seminar, September 22nd and 23rd, Bangalore, India

## Abstract:

With increasing complexity, shrinking size and high quality/low DPPB (Defective Part Per Billion) requirement for advanced automotive applications electronic test has become more challenging than ever. This two-day tutorial will systematically disseminate recent advances in electronic test to students, researchers and electronic test professionals. On Day 1, evolution of electronic test will be presented to set the context up for students and early career test professionals. Day 2 of tutorial will target seasoned researchers and mid-career and will cover advance topics like defect-oriented testing, test engineering standards and automotive testing. Lab session on Day 2 of tutorial will allow participants gleans hands-on on test logic insertion and validation.

**Nagesh Tamarapalli:**

Nagesh is an AMD Fellow with AMD India Design Center in Bangalore, India, where he leads a team engaged in high-quality manufacturing test for next generation microprocessors. The team's mandate spans the entire life cycle of DFT including architecture, implementation, verification, manufacturing test development, silicon bring up and diagnosis. Prior to AMD, he was with Mentor Graphics DFT group where he worked on logic BIST, test compression, and diagnosis tools. He has published several papers in leading test conferences and a paper he co-authored at International Test Conference 1999 on logic BIST has been recognized with "Honorable Mention Award". He is a co-inventor of 18 US patents in the area of testing. He has delivered DFT seminars at several venues including multiple VLSI Design Conference, ISQED 2007 and DAC 2008. He holds B.Tech. In ECE from REC Warangal, M.Tech. in Electrical Engineering from Indian Institute of Technology, Kharagpur, India, and Ph.D. in Electrical Engineering from McGill University, Montreal, Canada.

**Abhishek Chaudhary**

Abhishek Chaudhary is Manager, DFT Engineering at Rambus Bangalore. He has over 11 years of experience in DFT. He and his team are responsible for end to end DFT for all high speed SERDES and Memory PHY IPs across Rambus worldwide. He has also worked on DFT for automotive chips at Freescale Semiconductor (Now NXP) in the past. He holds patents and has published papers in reputed IEEE conferences and symposiums in India and abroad. He has completed BTech from VNIT Nagpur, MTech from IIT Delhi and is currently pursuing PhD from VNIT Nagpur.

**Sivanantham S**

Sivanantham is working as an Associate Professor in the School of Electronics Engineering, VIT University, Vellore, India. He worked as an Assistant Director for International Relations Office during 2014-15. He served as a Leader for VLSI and Embedded System Division at VIT University during 20072009. Previously he was associated with J.J. College of Engineering and Technology, Trichirappalli, India and Bannari Amman Institute of Technology, Satyamangalam, India as a faculty in the Department of Electronics and Communication Engineering. His area of research interest includes the design for testability, reconfigurable architectures, and low power VLSI design. He is the Senior Member of IEEE and member of IEICE, VLSI Society of India (VSI) and Indian Society for Technical Education (ISTE).

**Subhadip Kundu**

Subhadip Kundu is a Staff Engineer in DFT/ATPG team in Qualcomm India, Bangalore. He received his MS degree in Electronics Dept. in 2010 and PhD degree from Dept. of Computer Science and Engineering in 2014, both from IIT Kharagpur. His thesis work was shortlisted for TTTC thesis award and got a 3rd place at ATS 2014 chapter. Subhadip has published in more than 25 top international conferences and journals. He has best paper nomination at the 50th DAC 2012 and a best paper award at ARTcom, 2009. He has two US patents issued in the domain of VLSI diagnosis. He has worked in VLSI test research related topics such as power/thermal aware, ATPG, DFT, diagnostics for more than 10 years in academia and industry.

**Ankush Srivastava**

Ankush Srivastava received the Ph.D. from Indian Institute of Technology Bombay, Mumbai and the M.E. from the Birla Institute of Technology and Sciences, Pilani, India, all in Electrical Engineering. He is currently involved in enabling design-for-test (DFT) techniques for Qualcomm's state-of-the-art SoCs. Prior to this, he worked as DFT architect at NXP Semiconductors, India Design Center for 12 Years. He holds several international patents, journals and presented papers in various premier IEEE conferences. His current research interests include defining DFT architecture of complex SoCs, system security related to debug interfaces, effective and efficient small-delay defect-oriented test generation

**Prasad Mantri**

Prasad Mantri is Principal Engineer at the Microelectronics group at Oracle Systems group. He is involved in Design for Test, Microprocessor Test strategy, Test data volume and test time enhancement, Silicon yield analysis and yield debug, System failure analysis and debug as well as reliability and system product quality. He has worked at Sun Microsystem and Oracle Corporation for the past 13 years working on all their microprocessor designs. Before that, he has worked at Synopsys Inc, SGI, Micron and Silicon access. He has multiple papers and patents in logic and memory test. He has contributed to International Test Conference as a reviewer. He was on the organizing committee of ATE Vision 2020 conference. He has contributed to the ITRS Design and Test roadmap for multiple years as well as presented at the 3D IC design and test workshop organized by Sematec. He is a senior member of the IEEE and has contributed as a volunteer and is working on white papers on IEEE Internet Initiative. He has M Tech from IIT Madras

**Venkata Totakura**

Venkata is Design Engineering Director at Cypress Semiconductor Technologies. He is responsible for Chip Integration Center (CIC), implements Synthesis to GDS flow activities for various ASIC products of different Business Units such as Memory, Programmable SoC, Data Communication, and Automotive. He is New Product Development team member and responsible to develop and drive common ASIC implementation methodology across Cypress. He is DFT CoE (Centre of Excellence) quorum member and DFT-QA review board member at Cypress. He has Masters degree in VLSI CAD. He has 16 years of work experience in VLSI industry, worked for Mentor Graphics, Infineon and NXP organizations intensively into DFT domain. He authored/co-authored 10 papers in DFT and low power domains. He has an extensive experience in the field of ASIC design, implementation and successfully completed multiple Tapeouts in various technology nodes. He has been an active member in EDA standards, conferences and review committees. Venkata is an active member of ITC India committee and Tutorial Chairperson for ITC India conference consecutively for last 3 years.